Lesson 04: Functional units and components in a computer organization Part 3—Bus Structures
Objective:

- Understand the IO Subsystem and
- Understand Bus Structures
- Understand the functions of Data Address, Control and IO Buses
Memory Bus (System Bus)
Interconnection of Processor Functional units to memory and IO subsystem
Memory bus

• Memory bus (also called system bus since it interconnects the subsystems)
• Interconnects the processor with the memory systems and also connects the I/O bus
• Three sets of signals – address bus, data bus, and control bus
System Bus

• A system’s bus characteristics—according to the needs of the processor, speed, and word length for instructions and data
• Processor internal bus(es) characteristics differ from the system external bus(es)
Address, Data and Control Buses
Address Bus

• Through the address bus, processor issues the address of the instruction byte or word to the memory system

• Through the address bus, processor execution unit, when required, issues the address of the data (byte or word) to the memory system
32-bits Address Bus

- The address bus of 32-bits fetches the instruction or data from an address specified by a 32-bit number
Address Bus Example

- Let a processor at the start reset the program counter at address 0
- Then the processor issues address 0 on the bus and the instruction at address 0 is fetched from memory
Address Bus Example

- Let a processor instruction be such that it needs to load register r1 from the memory address M.
- The processor issues address M on the address bus and data at address M is fetched.
- From addresses M and M + 1 if bus width is 16 bits and memory stores 2 bytes for each word.
- From addresses M to M + 3 if bus width is 32 bits and memory stores 2 bytes for each word.
Data Bus

- When the Processor issues the address of the instruction, it gets back the instruction through the data bus
- When it issues the address of the data, it loads the data through the data bus
- When it issues the address of the data, it stores the data in the memory through the data bus
32-bit Data Bus

- A data bus of 32-bits fetches, loads, or stores the instruction or data of 32-bits at one time
Data Bus Example-1 of its use

• When the processor issues address \( m \) for an instruction, it fetches the instruction through data bus from address \( m \)

• For a 32-bit instruction, the word at data bus is fetched from addresses \( m, m + 1, m + 2, \) and \( m + 3 \)
Data Bus Example-2

- When an instruction is given to store register r1 to the memory address M, the processor issues address M on the bus and sends the data at address M through the data bus.
- For 32-bit data, word at data bus is sent to the memory addresses M, M + 1, M + 2, and M + 3.
Control Bus

- Issues signals to control the timing of various actions during interconnection
- Bus signals to synchronize the subsystems
Control Bus Signals

- Control signals as per the processor design
- Address latch ‘enable’
- Memory ‘read’
- Memory ‘write’
- IO ‘read’
- IO ‘write’
Control Bus Signals

• ‘data valid’
• **Interrupt acknowledge** on a **interrupt request** for drawing the processor attention to an event
• **hold acknowledge** on an external **hold request** for permitting use of the system buses
Control Bus Example 1

- When the processor issues the address, it also issues a *memory-read* control signal and waits for the data or instruction.
- Memory unit must place the instruction or data during the interval in which memory-read signal is active (not inactivated by the processor).
Control Bus Example 2

- Let the processor issue the address on the address bus, and after allowing sufficient time for the all address bits setup place the data on the data bus.
- Also then issues the memory-write control signal (after allowing sufficient time for the all data bits setup) for store signal to memory.
- The memory unit must write (store) the data during the interval in which memory-write signal is active (not inactivated by the processor).
IO Bus and PCI Bus
Devices on the I/O Bus

- Devices can be designed to interface with the bus, allowing them to be compatible with any computer that uses the same type of I/O bus.
Buses to interconnect the processor
Functional units to memory and IO systems
PCI bus interface

- In most systems, the processor has a single data bus that connects to a switch module such as the PCI bridge found in many PC systems
I/O Bus

• Allows a computer to interface with a wide range of I/O devices, without having to implement a specific interface for each I/O device

• Supports a variable number of devices, allowing users to add devices to a computer after it has been purchased
PCI Bus

- Almost all PCs and many workstations use the PCI bus standard for their I/O bus
- Can interface the systems to devices which are designed to meet the PCI standard
PCI Bus

- Almost all PCs and many workstations use the PCI bus standard for their I/O bus
- Can interface the systems to devices which are designed to meet the PCI standard
- All that required is a device driver for each operating system—a program that allows the operating system to control the I/O device
PCI bus interface

- The switch communicates with the memory through a *memory bus*, a dedicated set of wires that transfer data between these two systems.
- Some processors integrate the switch module onto the same integrated circuit as the processor to reduce the number of chips required to build a system and thus the system cost.
Downsides of using an I/O bus to interface to I/O devices

- All the I/O devices on a computer must share the I/O bus
- I/O buses are slower than dedicated connections between the processor and I/O device because the I/O buses are designed for maximum compatibility and flexibility
In most systems, the processor has a single data bus that also connects to a switch module such as the USB host controller found in many PC systems.

- Enables serial connection using limited number of lines to printer, scanner, digital camera, pen flash-drive
- Enables serial connection to USB wireless modem
Summary
We learnt

- Uses of the data, address, control and I/O Buses
- Uses of the PCI and USB Interfaces
End of Lesson 04 on
Functional units and components in a computer organization Part 3—Bus Structure