Chapter 13

PIC Family Microcontroller

Lesson 11

Capture of Timer Reading and interrupts using CCP1 and CCP2

Internal Peripherals

Synchronous Serial Port (MSSP)

10-bit ADC

USART

8-bit Timer TMR0

16-bit Timer TMR1

8-bit Timer TMR2

CCP1, CCP2

8

Flash Memory

13

Program counter

13

8-level stack (13-bit)

Data EEPROM 256 Byte

RAM Registers 368 Byte

Ports A to E

data bus

8
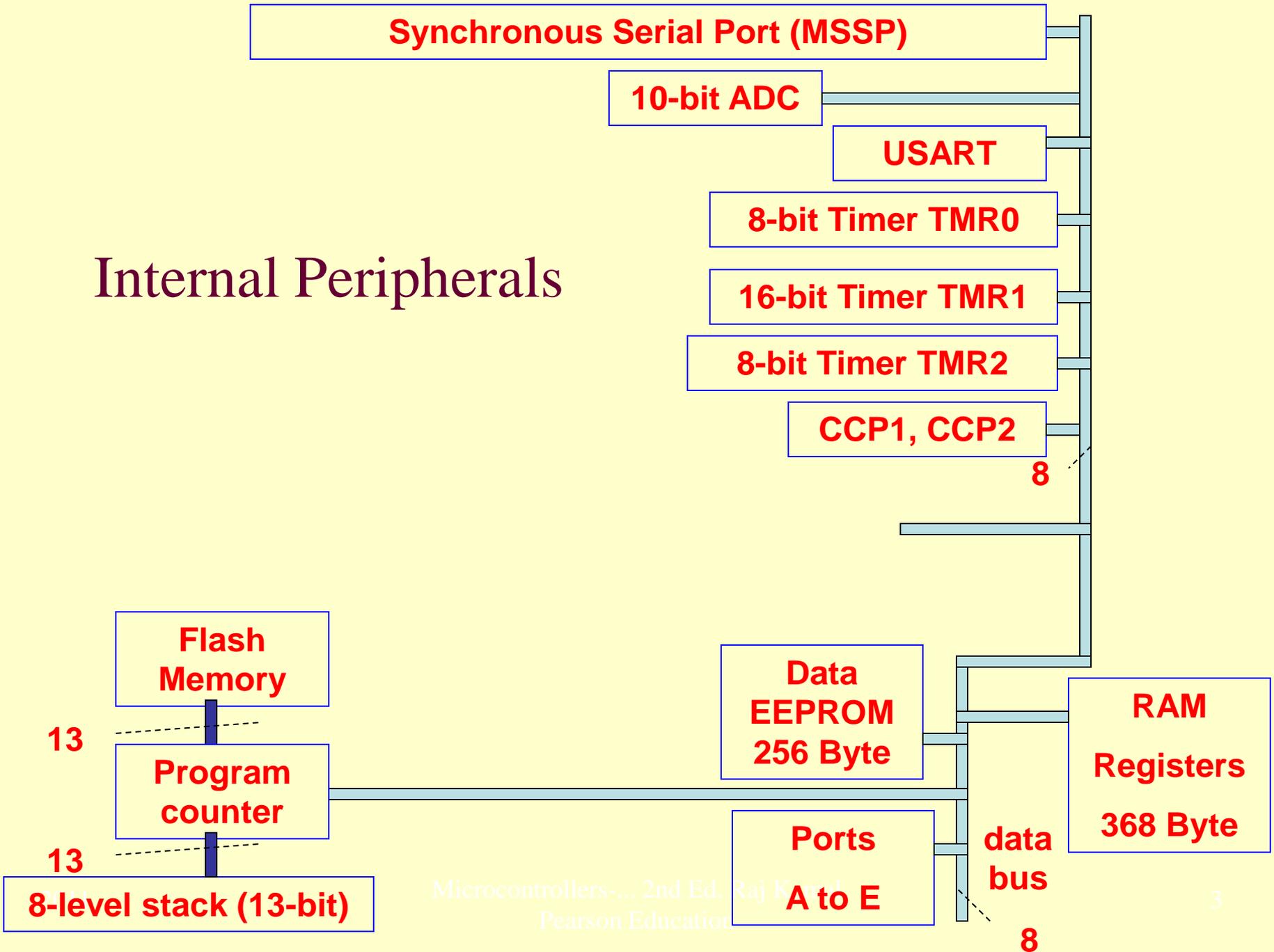
Capture Mode of CCP1 and CCP2

- When input is received at pin then CCPR1 captures (saves in CCPR1 register) the time (clock counts) in TMR1

- When input is received at other pin then CCPR2 captures (saves in CCPR2 register) the time (clock counts) in TMR1

Capture mode Registers Bank 0 Used

- CCPR1L-CCPR1H, CCP Register 1 lower and higher bytes at Bank 0 address 0x015-0x016
- CCP1CON for CCP1 control register at Bank 0 address 0x017
- CCPR2L-CCPR1H CCP Register 2 lower and higher bytes at Bank 0 address at 0x01B-0x01C
- CCP2 for CCP1 control at Bank 0 address at 0x01D

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Pins for CCP1 and CCP2 input

- RC1 functions as Capture 2 input to result in TMR1 counts capture in CCPR2L-CCPR2H when capture by CCP activated

- RC2 functions as Capture 1 input to result in TMR1 counts capture in CCPR1L-CCPR1H when capture by CCP activated

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CCP1 capture Mode

- Use 16-bit timer TMR1 for capturing the counts
- The time/counts at the holding register of TMR1— 16-bits at TMR1H:TMR1L
- TMR1H:TMR1L at address 0x0F-0x0E
- The bits used for capturing the 16-bits at CCPR1L:CCPR1H by the CCP1 device when CCP1 capture mode enabled
-

CCP2 capture Mode

- CCPR2H:CCPR2L 16-bit used in capture mode of CCP2

- CCP2 control register CCP2CON

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CCP2 capture Mode

- 16-bits at TMR1H:TMR1L time/counts at the holding register of TMR1

- TMR1H:TMR1L Bits used for capturing 16-bits at CCPR2L:CCPR2H by the CCP2 device when CCP2 capture mode enabled

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Using the CCP1CON bits

- Bit b7-b6 always 0 (not implemented in 16F877)

- Bit b5-b4 are not used in capture mode

- Bit b3-b2-b1-b0 = 1111 then capture/capture/PWM mode disabled

Using the CCP1CON bits b3-b2-b1-b0 = 0100

- = 0100 then capture mode activated
- CCP1 device captures a falling edge input (1 to 0 transition) at RC2 CCP1 pin and *writes on capture* (means 16-bits for the TMR1H:TMR1L counts are written at CCPR1L:CCPR1H)
- A flag CCP1IF (CCP1 interrupt flag) also sets
- The capture input at pin CCP1 (pin RC2 of PORTC)

Using the CCP1CON bits b3-b2-b1-b0 = 0101

- If = 0101 then capture mode activated
- CCP1 device captures a rising edge input (1 to 0 transition) at RC2 CCP1 pin and *writes on capture* (means 16-bits for the TMR1H:TMR1L counts are written at CCPR1L:CCPR1H)
- A flag CCP1IF (CCP1 interrupt flag) also sets
- The capture input is at pin CCP1 (pin RC2 of PORTC)

Using the CCP1CON bits b3-b2-b1-b0 = 0110

- If = 0110 then capture mode activated
- CCP1 device captures a every 4th rising edge (0 to 1 transition) input at RC2 CCP1 pin and *writes on capture* (means 16-bits for the TMR1H:TMR1L counts are written at CCPR1L:CCPR1H)
- A flag CCP1IF (CCP1 interrupt flag) also sets
- The capture iinput at pin CCP1 (pin RC2 of PORTC).

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Using the CCP1CON bits b3-b2-b1-b0 = 0111

- If = 0111 then capture mode activated
- CCP1 device captures a every 16th rising edge (0 to 1 transition) input at RC2 CCP1 pin and *writes on capture* (means 16-bits for the TMR1H:TMR1L counts are written at CCPR1L:CCPR1H)
- A flag CCP1IF (CCP1 interrupt flag) also sets
- The capture at pin CCP1 (pin RC2 of PORTC)

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CCP1IF (CCP1 interrupt flag)

- CCP1IF (CCP1 interrupt flag) is in SFR PIR1 (peripheral interrupt register 1) bit b2

- PIR1 address is 0x0C

- When CCP1IF (CCP1 interrupt flag) sets, the interrupt service routine executes

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Interrupt Execution on CCP1IF (CCP1 interrupt flag) Setting

- When Interrupt enabled by in SFR PIE1 (peripheral interrupt enable register 1) bit b2 and INTCON PEIE (peripheral-enable interrupts enable) bit b6
- PIE1 address 0x8C
- INTCON address 0x0B/0x8B/0x10B/0x18B

CCP2CON Bits

- CCP2CON bits at 0x1D are used as follows:
- Bit b7-b6 are always 0 (not implemented in 16F877)
- Bit b5-b4 are not used in capture mode
- B3-B2-B1-B0 used
- Bit b3-b2-b1-b0 = 1111 then capture/capture/PWM mode disabled

CCP2CON Bit b3-b2-b1-b0 = 0100

- = 0100 then capture mode activated
- CCP2 device captures a falling edge input (1 to 0 transition) at RC1 CCP2 pin and *writes on capture* (means 16-bits for the TMR1H:TMR1L counts are written at CCPR2L:CCPR2H)
- A flag CCP2IF (CCP2 interrupt flag) also sets
- The capture input at pin CCP1 (pin RC2 of PORTC).

CCP2CON Bit b3-b2-b1-b0 = 0101

- If = 0101 then capture mode activated
- CCP2 device captures a rising edge input (1 to 0 transition)at RC1 CCP1 pin and *writes on capture* (means 16-bits for the TMR1H:TMR1L counts are written at CCPR2L:CCPR2H)
- A flag CCP2IF (CCP2 interrupt flag) also sets
- The capture input at pin CCP2 (pin RC1 of PORTC).

CCP2CON Bit b3-b2-b1-b0 = 0110

- = 0110 then capture mode activated
- CCP2 device captures a every 4th rising edge (0 to 1 transition) input at RC21 CCP2 pin and *writes on capture* (means 16-bits for the TMR1H:TMR1L counts are written at CCPR1L:CCPR1H)
- A flag CCP2IF (CCP2 interrupt flag) also sets
- The capture input at pin CCP2 (pin RC1 of PORTC)

CCP2CON Bit b3-b2-b1-b0 = 0111

- If = 0111 then capture mode activated
- CCP2 device captures a every 16th rising edge (0 to 1 transition) input at RC2 CCP2 pin and *writes on capture* (means 16-bits for the TMR1H:TMR1L counts are written at CCPR2L:CCPR2H)
- A flag CCP2IF (CCP2 interrupt flag) also sets
- The capture is at pin CCP2 (pin RC1 of PORTC)

CCP2F (CCP1 interrupt flag)

- CCP2F (CCP1 interrupt flag) in SFR PIR2 (peripheral interrupt register 2 bit b0

- PIR2 address is 0x0D

- When CCP2IF (CCP2 interrupt flag) sets, the interrupt service routine executes

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CCPR2 Interrupt Service Routine Execution

- If interrupt is enabled by in SFR PIE2 (peripheral interrupt enable register 2) bit b0 and INTCON PEIE (peripheral-enable interrupts enable) bit b6.

- PIE2 address is 0x8D. INTCON address is 0x0B/0x8B/0x10B/0x18B.

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Summary

We learnt

- CCP1 and CCP2 Capture Modes

- Four Options Each

(i) Falling edge input at an RC pin and also Interrupt Flag set on capture

(ii) Rising edge input at an RC pin and also Interrupt Flag set on capture

(iii) Fourth Rising edge input at the RC pin and also Interrupt Flag set on capture at 4th edge

We learnt

(iv) Sixteenth Rising edge input at the RC pin and also Interrupt Flag set on capture at 16th edge

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End of Lesson 11 on

Capture of Timer Reading and interrupts using CCP1 and CCP2