Chapter 6

DIFFERENT TYPES OF LOGIC GATES
Lesson 3

RTL and DTL Gates
Outline

- **Resistor transistor logic (RTL)**
- RTL Circuit
- Characteristics of RTL gate circuit
- Diode transistor logic (DTL)
- DTL Circuit
- Characteristics of DTL gate circuit

RTL Input Stage and Basic Gate stage

• The two inputs connect to two n-p-n transistors through two ~ 450-Ohm resistances. That is why the name RTL.
• RTL circuit basic gate is two input NOR.
Output Stage for next stage input

• The common output F at the collector (s) of two n-p-n transistors at input stages is given to other resistances in the next stage RTL gates.
Outline

• Resistor transistor logic (RTL)

• **RTL Circuit**
  • Characteristics of RTL gate circuit

• Diode transistor logic (DTL)

• DTL Circuit
  • Characteristics of DTL gate circuit
Two Input RTL Circuit with two NPN Transistors

Logic NOR Circuit

Next stages
Cut-off region input

\[ I_B = I_C - I_E, \]
\[ I_B, I_C, I_E = \text{Negligible} \]
Saturation Region Case at input A or B

\[ I_B = I_C - I_E, \]
\[ I_B = \left( V_i - V_{BE \text{ (ON)}} \right)/R_B, \]
\[ I_C = \beta I_B = \beta \left( V_i - V_{BE(\text{ON})} \right)/R_B \]

The output at F is given by
\[ V_o = V_{CC} - I_C \cdot R \]
\[ = V_{CC} - R \beta \left( V_i - V_{BE \text{ (ON)}} \right)/R_B, \]
Either lower or upper transistor is at logic 1 input, the transistor operates in saturation region and output at F correspond to logic 0. Hence, RTL circuit functions as NOR gate.

- \( F = A + B \)
- Using NOR as building block other gates are made
Outline

- **Resistor transistor logic (RTL)**
- RTL Circuit
- **Characteristics of RTL gate circuit**
- Diode transistor logic (DTL)
- DTL Circuit
- **Characteristics of DTL gate circuit**
Wired ‘AND’

- B
- A
- C
- D

RTL Circuit-1

RTL Circuit-2

Permitted

F
Wired AND Two RTL gates

- F at two RTL gates interconnected, the output can be considered as AND operation between the logic outputs, because when both the outputs correspond to cutoff stages of the transistors, the output will remain unaffected and will be ‘1’. When any of the outputs correspond to saturation condition ~0.2V, the output from common point will become 0.2V. If A, B are the inputs at one RTL NOR gate and C, D are inputs at another, NOR the output will be as follows:

\[ F = (A + B). \overline{(C + D)} = (A + B + C + D) \]
Next Input Stages driven by output at F

- Base-Emitter Voltage, when a transistor is conducting (in saturation stage), is $V_{BE\ (sat)} = \sim 0.8V$. Base current for each output stage transistor $T_j \ (j = 1, \text{ will be } I_B = \frac{(V'_i - V_{BE\ (ON)})}{R_B} = \frac{1}{m} \frac{3.6V - 0.8V}{(640 \ \text{Ohm} + (450/m) \ \text{Ohm})} = V'_i$ is the input to $T_j$. 


Next Input Stages driven by output at F

- The collector current when this transistor is conducting (is in saturation) will be \( I_C = \frac{(3.6V - 0.2V)}{640 \text{ Ohm}} = 5.3 \text{ mA} \). A \( T_j \) transistor gain \( h_{fe} \) must be equal or greater than \( I_{C0} \) (saturation stage current) / \( I_B \). For \( m = 4 \), \( h_{fe} \geq \frac{(5.3\text{mA} / 0.93\text{mA})}{0.93\text{mA}} \) and \( h_{fe} \geq 5.8 \). \( h_{fe} \) = small signal current gain for the common emitter configuration.
Fan out

- For logic output of 1 at F, the output Voltage depends on \( m \) and \( m \) depends on the \( h_{fe} \) value of \( T_j \) transistor.
- Have more output stage transistors (\( j \) can be higher) if \( h_{fe} \) is higher. More output stage transistors means more output stages can be driven from the output F.
Propagation Delay

- Let base-emitter capacitance = \( C \) nF
  \([\text{nF means nanoFarad.}]\)
- If \( m = 4 \), the total capacitance being all \( T_j \) in parallel = \( 4C \).
- Resistance = \( 640 \text{ Ohm} + (450/m) \text{ Ohm} \)
  \( \text{Ohm} = 752.5 \text{ Ohm} \).
- Propagation delay = \( (640 m + 450) \text{ C ns} \)
  \([\text{nF} \times \text{Ohm} = \text{ns}]\)
Noise Margin at 0

- For logic state 0, the output at F can be ~0.2 V and maximum 0.5 V, else the T_j will start conducting and go in saturation. Hence **noise margin of logic state 0 in RTL based logic circuit is 0.3 V**
Noise Margin at 1

- We have seen that the output Voltage depends on $m$.
- For logic state 1, the output at $F$ can be calculated as follows:
  - Collector current at $T_j = 5.3$ mA for each transistor $T_j$, base current is $5.3\text{mA} / h_{fe} = 0.265$ mA assuming $h_{fe} = 20$
Noise Margin at 0 and at 1

For \( m = 4 \), total base current needed from \( F = m \cdot 0.265 \) mA = 1.06 mA.

Voltage at \( F = \) Voltage drop between T collector and emitter + total base current multiplied by total base resistance (450/m) Ohm. Thus Voltage at \( F \geq 0.8V + 1.06 \) mA. (450/m) ohm \( \geq 0.92 \) V
Noise Margin at 0 and at 1

- Available Output Voltage at F can be calculated as follows:

\[ V_O = 3.6 \text{ V} - \text{Voltage drop at (450/m) Ohm collector resistance} + \text{Voltage drop at 0.8 V base-emitter.} = 3.6V - \left( \frac{640 \text{ Ohm}}{640 \text{ Ohm} + 450/m \text{ Ohm}} \right) \times 0.8V = 1.2 \text{ V for } m = 4. \]
Noise Margin at 0 and at 1

- Hence the logic out 1 at F can be between the 1.2 V and 0.92V for $m = 4$ and $h_{fe} = 20$. For logic 1, noise margin will be 0.28V when $m = 4$ and $h_{fe} = 20$.
Outline

- Resistor transistor logic (RTL)
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- **Diode transistor logic (DTL)**
- DTL Circuit
- Characteristics of DTL gate circuit
DTL Input Stage and Basic Gate stage

- Two or more inputs to two or more n-ends of p-n diodes in place of passive 450-Ohm resistance in RTL circuit.
- Ref. Fig. for connections
Output Stage for next stage input

- A common output from the transistor T at F is given to other diodes at the other next stage(s) logic gates (DTL gates), which will get the input from the transistor, T
Outline

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Two Input DTL Circuit with one NPN Transistor

'1' \equiv V_{iA} > 3V_D^T

Logic NAND Circuit

Next stages

Cut-off region input

If $V_i$ A or B or C is low $\sim 0.2$ V then diode in the path conducts, $I_B$ through diode $\approx (5V - 0.7V - 0.2V)/5000\Omega = \sim 0.8$ mA. Voltage drop is 0.9 V and required for T base emitter to conduct is 1.4V. [0.7V is threshold voltage of one diode]

Therefore, $I_B$, $I_C$ and $I_E$ in T = Negligible

Any input 0, give output at F = 1, a characteristic of a NAND.
Saturation Region Case 1 at both input A and B

If both inputs A and B are high (>0.7V), the voltage at common p-ends will start exceeding 1.4V and the 2-diodes to the base will start conducting. When input A and B exceeds 1.4V and the voltage at the common p-ends exceeds \((1.4V + V_{BE}^{(ON)})= 2.1V\), the base-emitter junction starts conducting. Output at \(F = 0\) as expected from NAND.
Saturation Region Case at input A or B

When the A and B inputs exceed 1.4V, the diode stops conduction and when exceeds 2.1V, becomes reverse biased. $V_{BE\ (ON)}$ remains at 0.7V. If transistor T base-emitter current exceeds a limit, the T goes in saturation mode and it will start conducting current $I_C$ through R and $V_{CE} = \sim 0.2V$. Therefore, $F = 0$ when A and B both ‘1’
Output at F

Both A and B input at diodes and transistor are at logic 1 input, the transistor operates in saturation region and output at F correspond to logic 0. Hence, DTL circuit functions as NAND gate.

\[ F = \overline{A \cdot B} \]

Using NAND as building block other gates are made
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Wired ‘AND’

DTL Circuit-1

DTL Circuit-2

Permitted

F
Next Input Stages driven by output at F

- If the output from common collector junction is to $m$ number diode-transistor logic stage transistors, each driven through one input diode and 2-series diodes, the current from input stage is 0 from the F when all the next stage inputs are high.
Next Input Stages driven by output at F

- When a transistor T is conducting, the $V_{CE} = \sim 0.2 \text{V}$ (in saturation stage) and $V_{BE}^{(sat)} = \sim 0.8 \text{V}$. The currents from each output stage diode with the transistors $T_j$ ($j = 1, \ldots, j$) will be $mI_C$. The T will remain in saturation until the condition, $mI_C < \beta I_B$, $I_B = (2.1\text{V})/5000 \text{Ohm} = 0.4 \text{mA}$.
Fan out

- We can have more output D-T stages ($j$ can be higher) if $h_{fe}$ is higher. More output stages means more output stages can be driven through F. For logic output of 1 at F, the output Voltage does not depend on $m$. 
Fan out

Number of logic gates at the next stage(s) that can be loaded to a given logic gate output is the fan-out. Fan-out $m = \beta I_B / I_C$. 
DTL Circuit for increasing Fan out

‘1’ $\equiv V_{iA} > 3V_D^T$

$V_{iB}$

$V_{CE}$

5kΩ

2.2kΩ

$R^i_c$

$R_i$

$R_c$

$V^+_{CC}$

$F$

Logic NAND Circuit

$V_iB$

$A$

$B$

$+5V$

Ch06L3- "Digital Principles and Design", Raj Kamal, Pearson Education, 2006
Propagation Delay

- Let base-emitter capacitance = $C \, \text{nF}$ [nF means nanoFarad.] If $m = 4$, the total capacitance being all $T_j$ in parallel = $4C$. Resistance is very small between base and emitter in logic ‘1’ state. Therefore, transistor turn-on delay is small.
Propagation Delay

- Resistance in logic ‘0’ state is 5000 Ohm, therefore turn-off propagation delay = (5000) mC ns. [nF * Ohm = ns.] Typically, the turn-On delay is 30 ns and turn-off delay is 80 ns
Summary
Two types of Gates -

- RTL gate has each input connection to n-p-n through a resistance. It functions as NOR.
- DTL gate has each input connection through a pair of diodes or through a pair of transistor and diode to a common n-p-n transistor at output stages. It functions as NAND.
End of Lesson 3

RTL and DTL Gates
THANK YOU