Chapter 21

CPLDs and FPGAs
Field Programmable gate array (FPGA)

- No distinct input and output stages as in the AND-OR array and macro-cell, of a PAL and GAL, respectively.
Field Programmable gate array (FPGA)

- Logic cells
- All the logic cells arranged in the form, say, 12 x 8 or 24 x 32 matrix (array). A 12 x 8 FPGA possess total 96 logic cells. A 24 x 32 FPGA possess 768 logic cells.
- Uses CLBs (Configurable Logic Block) and LUTs (look-up based structure)
Characteristics Describing CPLD or FPGA

- Number of logic cells or macro-cells
- Technology for programming interconnects between inputs and outputs and between CLBs
- Whether long or single or both interconnects programmable
- Array structure
Logic Cells Array

Input-Output Blocks

A logic cell

A single interconnect

A long interconnect

An FPGA sub-array
Interconnects

- Dotted lines are single interconnects with programmable switches
- Dashed lines are long interconnects with programmable switches
Inter-connect

Inter-connect Line

From a SRAM cell

Inter-connect Line

Inter-connect Line

Inter-connect Line

Programmable MOSFET

a MUX input

da cell output
Inter-connect

- Inter-connect Line
- MUX Input
- Logic Cell
- AND array input
- From an SRAM Cell
- From an SRAM Cell
Anti-fuse Interconnect structure

Dielectric Layer

Poly-silicon

Insulator-semiconductor transition

n+
CLB (Configurable Logic Block)

- CLB is a matrix with single length interconnects
- Row based architecture with single length Interconnect
- Hierarchical Structures
IO Block Inter-connects

- Connect by long inter-connects
- Connects the CLBs through single inter-connects and long interconnects
Logic cell

- A combination circuit input stage for SOPs plus a macro-cell designed in a much more flexible way with (i) Feedback possibilities not only from a neighbouring IO stage but from other stages as well, and (ii) provision of multiple outputs from a macro-cell.
A logic cell consists of the followings:
(i) Gates to implement SOP function,
(ii) D- FF with preset and clear, and
(iii) Data path selector —multiplexer (MUX) at the input.
Array of Cells

- 100 to 750 cells in a single EPLD IC for implementing FPGA
- (i) The number of IO (input and output) pins could be 50 to 200
- (ii) Number of clock inputs can be 8, and
- (iii) Number of gates (NANDs or NORs) could be from 1000 to 50,000.

[Note: Xilinx has done pioneering work. A latest FPGA XC2VP125 has 125136 logic cells.]
A logic cell

• (i) two number six inputs AND gates, four number two input AND gates, three number 2 to 1 MUXs and a clock input edge triggered D FF with the preset and clear inputs, and

• (ii) three number outputs from the ANDs, one output from the MUX and one output from the D FF.
A logic cell

• Per logic cell, the total number of inputs are 21 and outputs are 5. We can not only obtain SOP functions on the inputs but also the multiplexing and decoding functions at the inputs at the logic cell.
A logic cell design

- Each cell arranged as an element in a matrix inside
- FPGA facilitates implementation of a multiple bits (16 or 32) complex combinational or sequential circuits
A logic cell design

- The examples are an adder or other arithmetic unit, a state machine, a shift register or an auto re-loadable counter.
A logic cell design

- D-FF in a cell of the FPGA configurable as JK FF, RS FF or T FF, which facilitates an implementation of the 16 or 32 bit circuit for the various types of the shift registers and counters
LUTs for Programming the cells

- LUT (Lookup table)
- A table of inputs and outputs
- Inputs are for a key
LUTs for Programming the cells

- LUT in an FPGA — $2^m \times 1$ bit memory unit
- Interconnect switches are programmed to connect cell inputs through the LUTs or directly to the MUXs and other gates of a cell
Example of applications

- Data acquisition logic, plant automatic operation controller, graphic or image or voice processor, mouse interface, disk cache controller or parallel processor controller or encryption device, decryption device, pattern recognizer, DNA sequence storage, signature recorder
Summary
• FPGA is an array of programmable CLBs (configurable logic blocks)
• Each CLB has IO blocks
• Each IO block has logic cells
• Logic cells have MUXs and D-FF with S and R inputs (usable as T, RS and JK)
• SRAM based inter-connects
• Interconnects are programmable fusible links
SRAM based inter-connects

Interconnects are programmable fusible links
End of Lesson 2

FPGAs
THANK YOU