Chapter 18

FUNDAMENTAL MODE SEQUENTIAL CIRCUITS

Lesson 1

General Asynchronous Sequential Circuit with the memory section with latches and combinational circuits at input and output stages

Outline

- **Two Classifications of Sequential Circuits - Synchronous and Asynchronous**
- General Asynchronous sequential circuit
- Unstable Operation
- Fundamental mode operation
- Tabular Representation of Excitation-cum-Transitions of States and outputs

Synchronous sequential circuit

- A circuit in which the output **Y** depends on present state **Q** and present inputs **X** at the clocked ↑ or ↓ or ⎍ (MS) or ⎏ (MS) instance(s) only.

Memory Section

- Memory section activates a transition as per the excitation inputs to the next state **Q'.** A clock input (or a set of inputs is used) to cause a transition to next state.

Asynchronous sequential circuit

- A circuit in which not only the present inputs **X** and present state **Q** but also the sequences of changes affect the output **Y**. Asynchronous means that the changes can be at the undefined instances of time.
- There are no controls for the instance(s) at which output(s) changes

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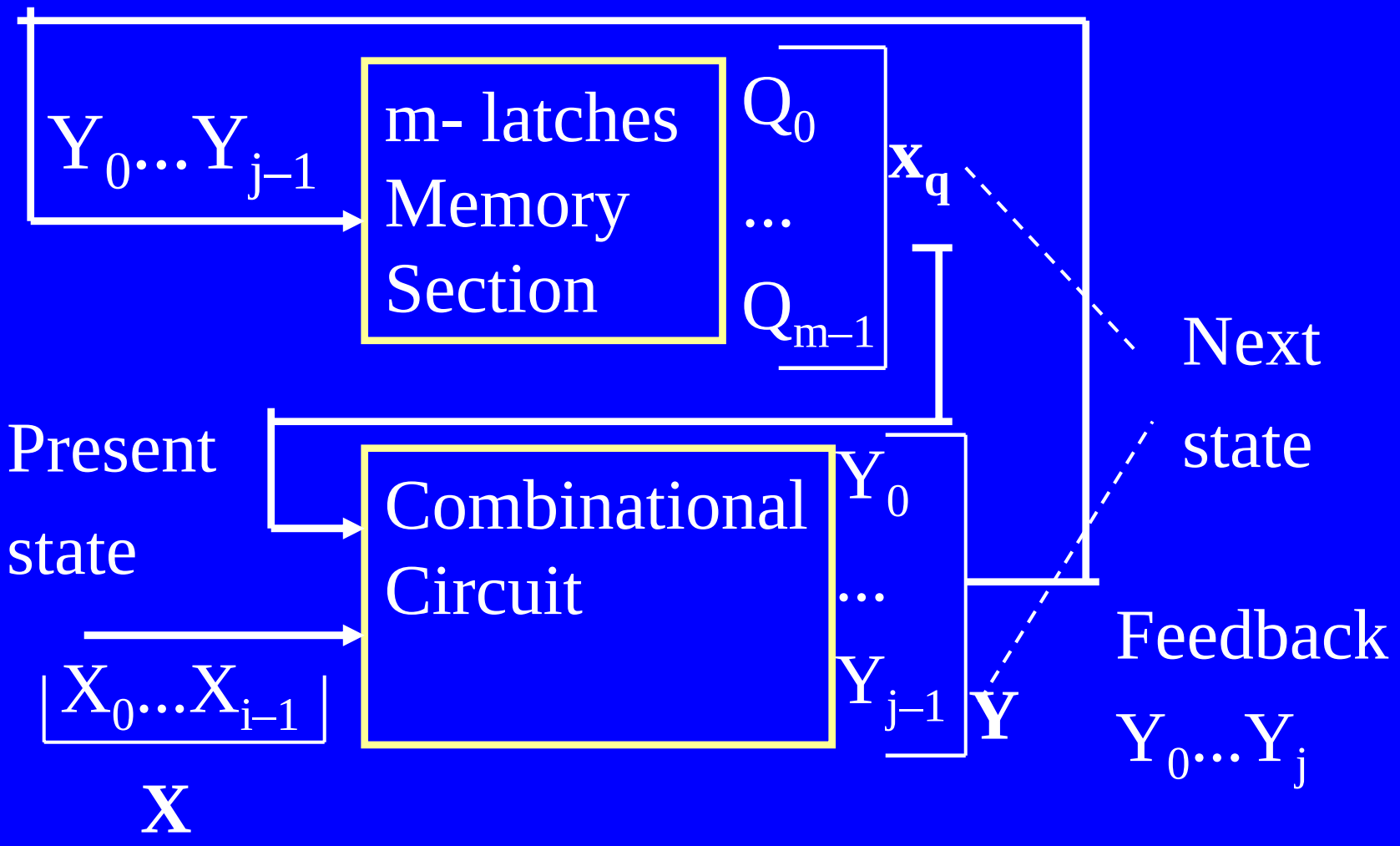
General asynchronous sequential-circuit

- Has a section consisting of the (i) latches without clock inputs (or an equivalent delay device) and the (ii) combinational circuits at input and output stages.
- It means memory section of clocked sequential circuit replaces the latches without clock inputs (or an equivalent delay device).

General Asynchronous Sequential Circuit



Memory Section Output **Q**

- *m* of latches without clock edges or pulses to control instances of transitions
- Section output is set $\mathbf{x_q}$. $\mathbf{x_q}$ has *m* present-state outputs —$x_{\mathbf{q}0}$, $x_{\mathbf{q}1}$… and $x_{\mathbf{q}m-1}$, which appears after a delay arising from the latches when section input set $\mathbf{y_q}$ applies. $\mathbf{y_q}$ has *m* inputs inputs —$y_{\mathbf{q}0}$, $y_{\mathbf{q}1}$… and $y_{\mathbf{q}j-1}$

External Input $\underline{X}$ and present state x_q(**x_{q0}, x_{q1}… and x_{qm-1}**) inputs to a combinational circuit

- Set $\underline{X}$ of *i* inputs — X_0, X_1, ...X_{i-1}.
- Set x_q m inputs, which are x_q outputs of memory section
- Both $\underline{X}$ and x_q are the combinational circuit inputs

Outputs $\underline{\mathbf{Y}}$ from the combinational circuit with $\mathbf{x_q}$ and $\underline{\mathbf{X}}$ in the inputs

- A Set $\underline{\mathbf{Y}}$ [= *i* outputs — $Y_0, Y_1, \ldots Y_{i-1}$] out of which a subset $\mathbf{y_q}$ **[**= $Y_0, Y_1, \ldots Y_{j-1}$] is feedback as input to memory section to get next state.

➢ Note: Sequential circuit is one the present state **Q** is input to have transition to next state **Q'.**

State Machine

- A sequential circuit can also be considered as a machine producing states after undergoing sequential transitions
- Instances of Sequence change is not guided in asynchronous sequential circuits

State Machine without clock-control

- A sequential asynchronous circuit is also like a machine producing ***states*** without a clock controlling them.

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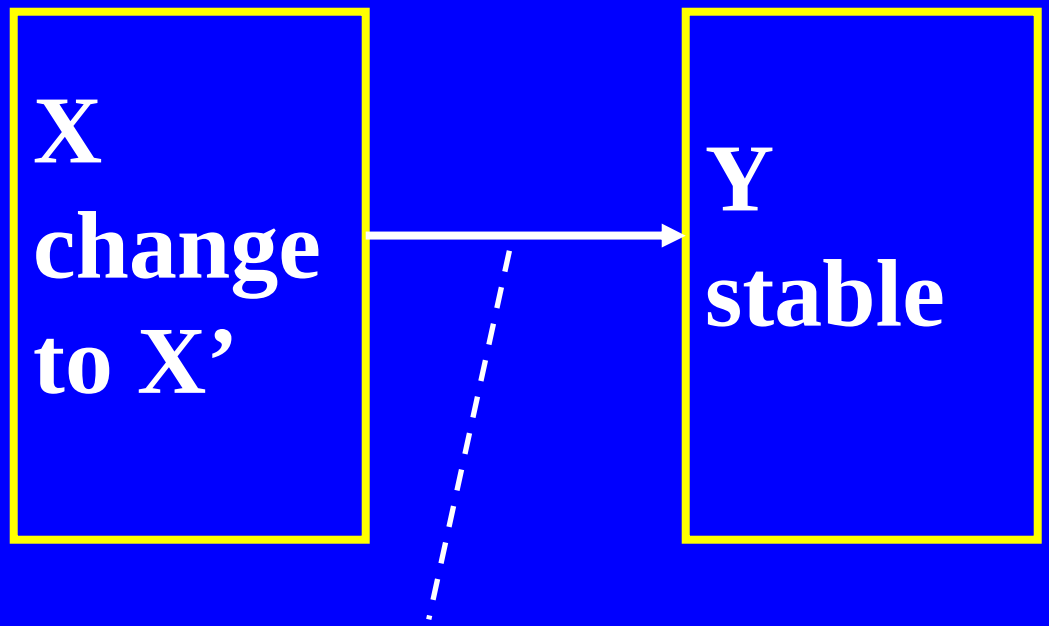
Unstable General Circuit



n Cycles Taken for stability.*n* can be 0 (stable in first feedback cycle) to infinity (never stable)

Asynchronous sequential circuit

- Step 1:Let us assume that the input change applied only at stable $\underline{x_q}$. Let the present state $\underline{Y_0}$ and therefore its subset $\underline{y_{q-}}$ changes when a bit changes $\underline{X_k}$ to $\underline{X'_k}$. Therefore, $\underline{Y_0}$ changes to $\underline{Y}$ after a normal gate propagation delays (not in consideration).

Asynchronous sequential circuit

- Step 2:In the first feedback-cycle, a delayed change in $\underline{x_q}$ occurs due to change in $\underline{y_q}$ to $\underline{y'_q}$, being a subset of $\underline{Y}$. The feedback $\underline{x'_q}$ after a memory-section delay combined with $\underline{X_i}$ changes $\underline{Y}$ to next state $\underline{Y'}$.

Asynchronous sequential circuit

- Step 3:In next feedback-cycle a delayed change in x'_q may also occur due to change to y'_q, a subset of Y'. The feedback x''_q after the feedback-cycle of delay combined with X_i may therefore change Y' to next state Y''.

Asynchronous sequential circuit Instability

- After Step 2 feedback-cycle, if there are changes to the next state(s), the **Y** is said to be unstable till after in any further feedback-cycle there is no change

Asynchronous sequential circuit Stability after a few cycles or after infinity

- If after first feedback-cycle or an (n + 1)th feedback-cycle, if the Y does not change, then the circuit is said to become stable. The *n* can be 0 to infinity; the circuit can be permanently unstable.

Example of Circuit - *i* as asynchronous unstable sequential circuit

- Circuit-*i* remains unstable in successive feedback-cycles, when X_0 change from 0 to 1. Let instant when X0 changes from 0 to 1 when there is stable x_Q = 1. The buffer gives the output y0 =1 and y1 = 1. The y1 in first feedback-cycle after a delay gives the output = x'_Q = 0.

Unstable till Infinity Circuit-*i*

- Therefore, now y1 now becomes y'1 and is 0. Now when y1 = 0, the x''_Q will become = 1. The x_Q continues to toggle after successive delays. The circuit is unstable till infinity

Unstable circuit condition

- Asynchronous sequential circuit is called unstable when the next state changes repeatedly without settling to a stable state.

Stable circuit condition

- Asynchronous sequential circuit is called a stable circuit when after an input change the next settles to a stable state in first or known number of feedback-cycles in memory section (or latches).

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- **Fundamental mode operation**
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Definition of Fundamental Mode Circuit

- Fundamental mode of an asynchronous sequential circuit is a mode in which input changes only when the circuit is in stable state.

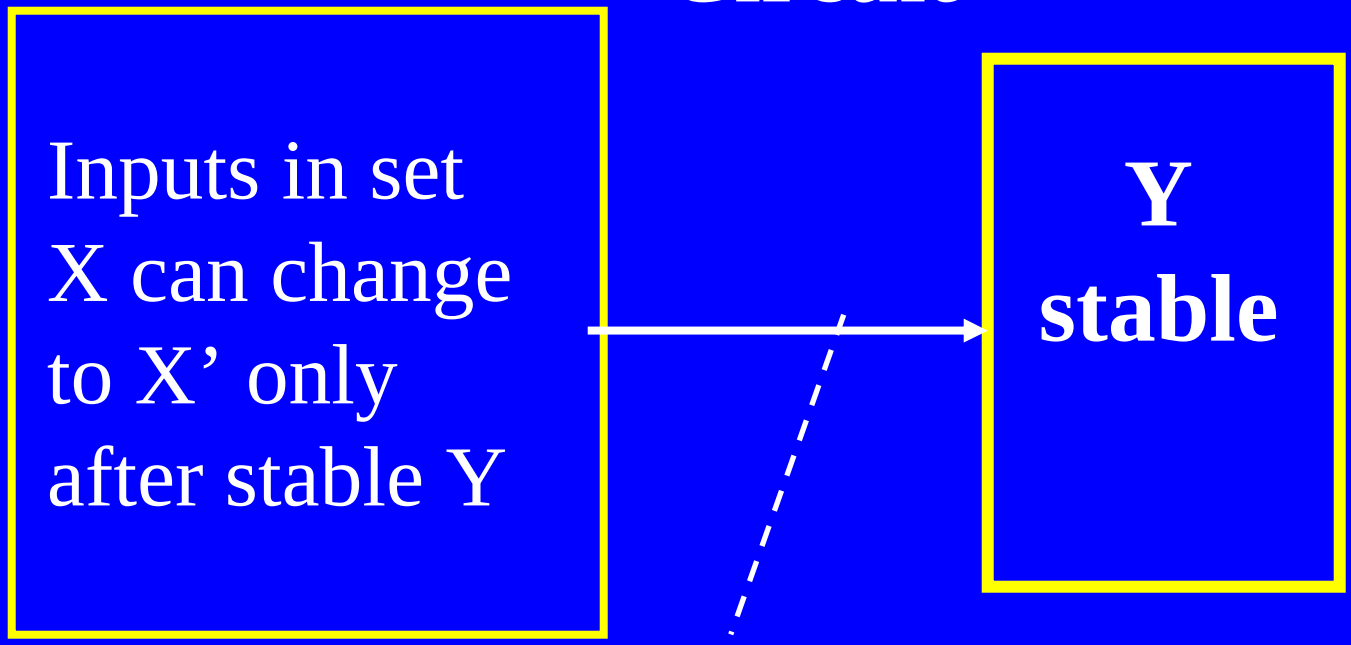
Fundamental Mode

- Asynchronous sequential circuit operates as a fundamental mode operating circuit when no input variable(s) $\underline{\mathbf{X}_i}$ is changed unless the $\underline{\mathbf{x}_q}$ and $\underline{\mathbf{y}_q}$ are stable.

Fundamental Mode Circuit Special case

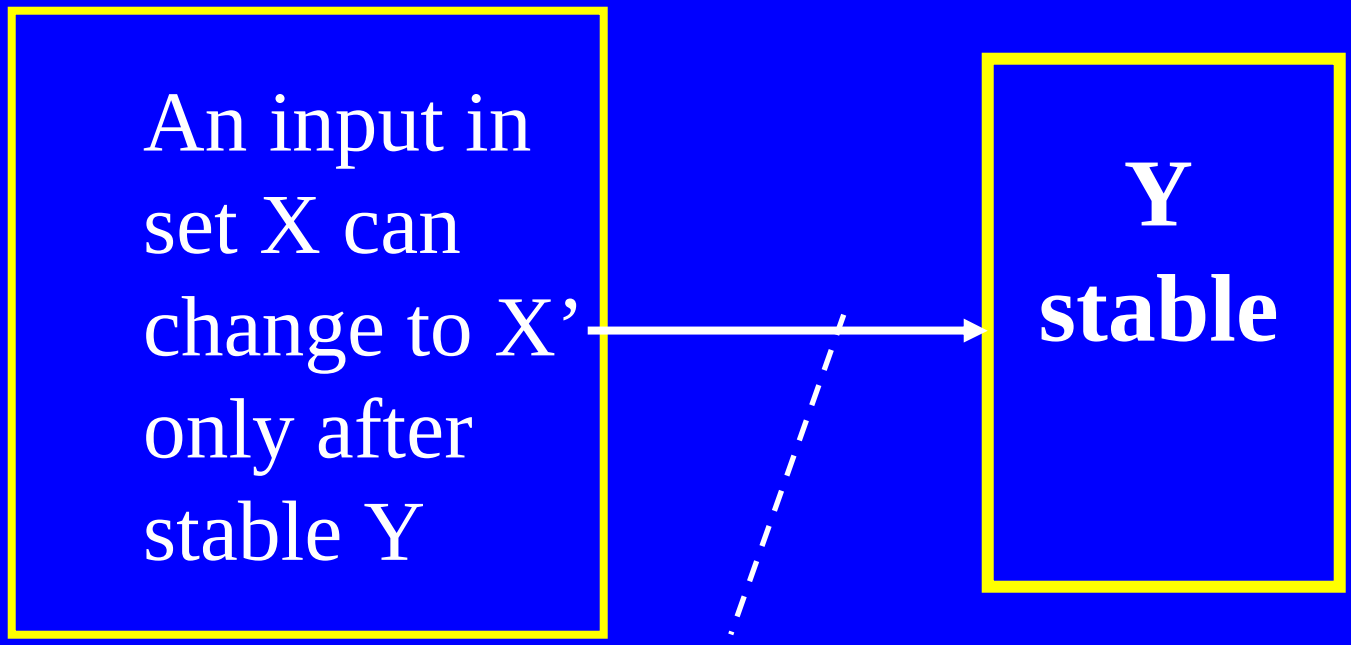
- A special case of fundamental mode circuit is useful for an analysis of fundamental mode circuit and is that only one input variable (one input bit) change at an instance for changing one state of $\underline{Y_0}$ to the next state of $\underline{Y}$.

Asynchronous sequential circuit operation as Fundamental Mode Circuit



n Cycles Taken for stability.*n* can be 0 (stable in first feedback cycle) to infinity (never stable)

Special Case of asynchronous sequential circuit: Fundamental Mode Circuit with one input change at a time



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Representation of transitions instability and final stable state in Excitation-cum-Transition Table

- Finally becoming stable state shown in the table by having a circle or square over it
- Horizontal and vertical directed arcs in the table show action of combinational and memory section circuits

Representation of transitions

- Stable state is marked by circle or ellipse over the state variables or state name.
- Horizontal directed arc(s) with arrow shows the action at the combinational circuit.
- Vertical directed arc(s) with arrow shows the action at the memory section by latches.
- Number of vertical arcs equal the number of feedback-cycles after which stability is achieved

Excitation-cum-Transition Table for Y = $\overline{X}.\ x_{q2} + x_{q1}$;

$x_{q1}' = D$ and $x_{q2}' = x_{qn+1} = J.\ \overline{x}_{q\,n} + \overline{K}.\ x_{q\,n}$

State	Transition Outputs		Y	
(Q_1, Q_2)	$[Q1', Q2']_{X=0}$	$[Q1', Q2']_{X=1}$	X=0	X =1
(0, 0)	0, 0	1, 0	0	0
(0, 1)	0, 1	1, 0	1	0
(1, 0)	0, 1	1, 1	1	1
(1, 1)	0, 1	0, 0	1	1

Delay Section Inputs

- $D = y_{q0}$
- $J = y_{q1}$
- $K = y_{q2}$

Combinational Circuit Inputs

- X = 0 or 1
- $x_{q1} = D = y_{q0}$ after a delay
- $\overline{x}_{q2} = J.\, x_{q2} + \overline{K}.\ \overline{x}_{q2}$ after a delay

  $= y_{q1}.\, x_{q2} + \overline{y}_{q2}.\ \overline{x}_{q2}$ after a delay

Combinational Circuit Outputs

- $Y_0 = \overline{X} \cdot \overline{x}_{q2} \cdot + x_{q1}$
- $y_{q0} = X \cdot (x_{q2} + \overline{x}_{q1}) = D$
- $y_{q1} = x_{q1} = J$
- $y_{q2} = K = X$

Summary

- Asynchronous Sequential circuit has both the memory section and combinational circuit, and memory section has no clocked instances or clock inputs
- Output change in first feedback cycle through memory section, then in second, ...

- Out is stable in $(n+1)^{th}$ cycle, where n= 0 to infinity
- Fundamental mode operation, the external inputs can change only after stable state is reached from previous inputs.
- Analysis is easy with the assumption of only one input change at a time

- Excitation cum Transition Table shows the ellipse or rectangle over the stable state and shows combinational circuit effects by horizontal arcs and memory section feedback cycle effects by vertical arcs.

End of Lesson 1 on

General Asynchronous Sequential Circuit with the memory section with latches and combinational circuits at input and output stages

THANK YOU