Chapter 17

RAM, Address and Data
Buses, Memory Decoding,
Semiconductor Memories
Lesson 3

Internal Address Decoding and RAM ICs
Outline

- Internal address decoding
- IC for RAM
Memory Cell Arrays of 8 Bytes

Cell array has similar functions, as IO buffer registers

Data Common Lines (Data Bus)

Write Enable
Read Enable

2^{16} Memory Cell Arrays of 8 Bytes

Cell array has similar functions, as IO buffer registers.

Data Common Lines (Data Bus)

Write Enable

Read Enable

Chip Select

Address Bus

Address Decoder

CA 2^{16} – 1

CA1

CA0

A15

A1

A0
Horizontal and Vertical decoders

- Internal Decoders

  i-bits of Address Bus

  Number of bytes accessed = $2^{i+j}$

- Vertical Address Decoder

  j-bits of Address Bus

- Horizontal Address Decoder
Decoder Tree

- Horizontal and vertical decoders help in accessing one of \(2^i + j\) cell-arrays using \(2^i + 2^j\) internal lines in place of \(2^{i+j}\) internal lines.
- In place of horizontal and vertical decoders for the cell arrays of RAM, a decoder tree can be used. Decoder tree further simplifies the circuit by having fewer internal lines.
Outline

- Internal address decoding
- **IC for RAM**
2k × 8 RAM Integrated Chip IC 6116

- 2k means $2 \times 1024 = 2 \times 2^{10}$ addresses = $2 \times 2^{10}$ cell-array
- × 8 means each memory-cell array has 8-bits
- 8-bit Data bus required
- 10-bit address bus required
IC 6116

**RAM**

6116

2k \times 8 \text{ RAM}

8-bit Data Bus

10-bit Address Bus

Chip Select

Write Enable

Read Enable

3 Control Signals

1 M × 8 RAM Integrated Chip IC

- 1 M means $2 \times 1024 \times 1024 = 2 \times 2^{10} \times 2^{10}$ addresses $= 2 \times 2^{20}$ cell-arrays
- \( \times 8 \) means each memory-cell array has 8-bits
- 8-bit Data bus required
- 20-bit address bus required
IC 1 MB RAM

RAM

1M × 8 RAM

20-bit Address Bus

Chip Select

Write Enable

Read Enable

3 Control Signals

8-bit Data Bus
Cell array has similar functions, as IO buffer registers.

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2^{20} Memory Cell Arrays of 1 MB RAM

- Address Bus
- Chip Select
- Read Enable
- Write Enable
- Data Common Lines (Data Bus)
- CA \(2^{20}-1\)
- CA0
- CA1
- Decoder

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Summary
- An internal decoder tree selects a byte in the IC chips
- IC chip have large memory
- RAM chip has 8-bit data bus, m-bit address bus and control signals. m-bit bus addresses $2^m$ bytes
- Control signals —chip select, read and write
End of Lesson 3

Internal Address Decoding and RAM ICs
THANK YOU