Chapter 16
Sequential Circuits for Registers and Counters
Lesson 2

Shift Registers
Outline

- **Shift Register**
- Serial-In Serial-Out Register
- Serial-In Parallel-Out Register
- Parallel In Serial Out Shift Register
- Parallel In Parallel Out Shift Register
4-bit Shift Register

- A shift register is a clocked sequential circuit in which stored the binary word bits shift either towards left or towards right (towards higher place value or lower place value) on each successive clock transition.
4-bit Right Shift Register \((n+1)^{th}\) clock transition after \(n^{th}\) clock defined the present state

- Serial input \(\rightarrow Q_A\);
- \(Q_A \rightarrow Q_B\);
- \(Q_B \rightarrow Q_C\);
- \(Q_C \rightarrow Q_D\);
- \(Q_D = \) Serial out;
- when output bits from left to right are \(Q_A, Q_B, Q_C\) and \(Q_D\).
4-bit Left Shift Register \((n + 1)^{\text{th}}\) clock transition after \(n^{\text{th}}\) clock defined the present state

- \(Q_D \leftarrow\) Serial input;
- \(Q_C \leftarrow Q_D\);
- \(Q_B \leftarrow Q_C\);
- \(Q_A \leftarrow Q_B\);
- \(Q_A =\) Serial out
- when output bits from right to left are \(Q_D, Q_C, Q_B\) and \(Q_A\).
Average Propagation Delay in Shifting at outputs

- Average propagation delay, $t_p$ of a Register is average interval $t_p$ from the +ve or -ve edge of CLK (Shift-clock) after which $Q_A.. Q_D$ get the new values $Q'_A.. Q'_D$
Clock Edges

- Shift register “looks upon” the data bits at $D_D$, $D_C$, $D_B$, $D_A$ inputs (= Qs of previous state only) at the instant of a falling edge (-ve edge) in case of -ve edge D-FFs are used and at rising edge in case +ve edge D-FFs are used.
Outline

- Shift Register
- **Serial-In Serial-Out Register**
- Serial-In Parallel-Out Register
- Parallel In Serial Out Shift Register
- Parallel In Parallel Out Shift Register
4-bit Right Shift Register SISO using D-FFs

4-bit Q Internal FF-Outputs

Serial-in

D

CLK (shift)

D

Q_{A}

D-FF

D

Q_{B}

D-FF

D

Q_{C}

D-FF

D

Q_{D}

D-FF

Serial-Out

4-bit Left Shift Register SISO using D-FFs
Timing Diagram when +ve edge Clk D-FFs Right shift SISO

CLK (shift)

1 or 0 Serial in

QA
QB
QC
QD Serial out

t

Timing Diagram when +ve edge Clk D-FFs Left shift SISO

CLK (shift)
1 or 0 Serial-in

Q_A Serial out
Q_B
Q_C
Q_D
Shift Register

- A shift register shifts the transfers the input D bits to next Qs such that $Q'_i (n+1) = D_i$ after an interval from $n^{th}$ clock edge instance plus propagation delay.
Average Propagation Delay from input at one end to FF to last end FF Q output

• Average propagation delay, $t_p$ of a Register is 4-times the average interval $t_p$ from the +ve or -ve edge of CLK (Shift-clock) after which $Q_A.. Q_D$ get the new values $Q'_A.. Q'_D$
Outline

• Shift Register
• Serial-In Serial-Out Register
• Serial-In Parallel-Out Register

Parallel In Serial Out Shift Register
Parallel In Parallel Out Shift Register
4-bit Right Shift Register SIPO using D-FFs
4-bit Left Shift Register SIPO using D-FFs

State Table for SIPO

- Refer Text
Outline

- Shift Register
- Serial-In Serial-Out Register
- Serial-In Parallel-Out Register
- Parallel In Serial Out Shift Register
- Parallel In Parallel Out Shift Register
4-bit Right Shift Register PISO using D-FFs; L/S means load when 1 and shift when 0.

4-bit left Shift Register PISO using D-FFs; L/S means load when 1 and shift when 0.
State Table and State Diagram for PIPO

- Refer Text
D-FF from RS FFs

- RS FFs are used for PISO
- R connects CLR input. When CLR = 0, then all Qs become 0
- Each R connects to S through a NOT gate
- Each D input is at S input
- Each X input is at AND. Other input of AND connects Load/Shift (L/\bar{S}) line.
Outline

• Shift Register
• Serial-In Serial-Out Register
• Serial-In Parallel-Register
• Parallel In Serial Out Shift Register
• **Parallel In Parallel Out Shift Register**
CLK (shift) Serial- Out at QA

Left Shift PIPO

L/S

Q_A

PR

D-FF

S

R

PR

D-FF

S

R

PR

D-FF

S

R

PR

D-FF

S

R

D

CLR

OE

Y_A

Y_B

Y_C

Y_D

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Q_A

Q_B

Q_C

Q_D
A parallel in parallel out (PIPO) Shift Register

- Transfers the input bits $X$ to next $Q_s$ such that $Q'_i(n+1) = X_i$ after $n^{th}$ clock input.
- Loads the external inputs as the excitation inputs through ANDs.
- Shifts on transition to the next state on a clock transition.
A parallel in parallel out (PIPO)

- Gives parallel outputs $Y_i$ through ANDs, which are the same as the next state. [Parallel Outputs mean $Y_i = Q'_i$ and Parallel inputs mean $X_i = D_i$ at same time where $i = 0, 1, 2$ or $3$ for a 4-bit PIPO. Note: $i = 0, 1, 2... n-1$ in an $n$-bit PIPO register]
A parallel in parallel out (PIPO) Shift Register

- Applied all n-inputs Xs on n-parallel input lines, called parallel load lines. Inputs load when L/S = 1
- All n-outputs Qs are on parallel lines.
- Qs Shift on L/S = 0
- Ys outputs on OE = 1
Summary
• Four type of Shift registers
• SISO
• SIPO
• PISO
• PISO
• Register shifts the inputs on clock edge because Q-input of one stage FF connects to D-input of next stage FF
• Left most D-FF input is serial input for right shift register
• Right most D-FF input is serial input for left shift register
• Left most D-FF output is serial output for left shift register
• Right most D-FF output is serial output for right shift register
End of Lesson 2 on
Shift Registers
Thank You