Chapter 14

Sequential logic, Latches and Flip-Flops
Lesson 2

Sequential logic circuit, Flip Flop and Latch— Introduction
Outline

- **Sequential logic circuit**
  - Clock input
  - Propagation delay, and Setup and hold times
  - Flip Flop
  -Latch
Example— Basic unit of Combinational Circuits

- Gates
- Mux
- decoder
- PROM
- PAL (unregistered)
Example— Basic Sequential Circuits

- FF — SR, JK, D, T
- Latch
- Counter
- Register
Sequential Action

• Sequential action means (i) to remember what steps are to be done next, and (ii) to recall which step has just been finished
Definition

• A sequential circuit is a circuit made up by combining logic gates such that the required logic at the output(s) depends not only on the current input logic conditions but also on the past inputs, outputs and sequences.
Sequential Circuit State Table

- Sequential circuit has a state table (like truth table in a combinational circuit)
- Sequences are specified by a table called state table.
- State table gives the past, current and future states at the output.
Sequential Circuit Features

- Sequential circuit has a feedback of the output(s) from a stage to the input of either that stage or any previous stage.
Sequential Circuit Features

- An output depends on the current input state and past input state (thus past output state)
- An output(s) can remain stable (constant) even after the input conditions change
Sequential circuit feature

- An output(s) at each stage appears after a delay of few tens or hundred ns depending upon the gate type or family of used to implement the circuit
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Sequential Circuit Features

- A sequential circuit may have a clock (gate) input to control the instance or time interval in which the output gets affected as per the inputs to the sequential circuit and in which the output undergoes transition to next state.
Clock Input

- Input after which the state at output(s) of sequential circuit undergoes transition to next state
Clock Input

- Asynchronous input (Level clocking) — A time interval defined by clock input during which input changes reflect on the output
- Level means 1 for a time interval or 0 for a time interval
Clock Input

- Synchronous input — (i) Edge +ve or –ve defines the instance at which input affects the output and transition is to next state (ii) Master slave — at +ve edge at master section of circuit, there is transition at master’s output and at –ve edge, the slave output undergoes transition as per master output.
+ ve edge and -ve edge

- + edge means transition at input from 0 to 1
- - edge means transition at input from 0 to 1
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Propagation Delay 0 to 1 transition

- Propagation delay, $t_{p(01)}$ or $t_{p_{LH}}$ is the time interval between $t'$ and $t''$, where $t'$ is the instance midway between 0 and 1 when a sequential circuit input is changing from 0 to 1 and $t''$ is the instance midway between 0 and 1 when an output $Q$ is changing from 0 to 1
Propagation Delay 1 to 0 transition

- Propagation delay, $t_{p(10)}$ or $t_{pHL}$ is the time interval between $t'''$ and $t''''$, where $t'''$ is the instance midway between 1 and 0 when an input is changing from 1 to 0 and $t''''$ is the instance midway between 1 and 0 when the output Q is changing from 1 to 0.
Average Propagation Delay

• Average propagation delay, $t_p$ of a latch or FF is the average of $t_p(01)$ and $t_p(10)$. [The delays $t_p(01)$, $t_p(10)$ and $t_p$ differs due to different impedances of the output stage transistor.] These also depend on the types and family of the gates used in designing an FF
Setup Time

- Setup time, $\bar{t}_s$ is an average of the minimum required time for input before enabling input (gate input or clock input) is applied so that the output $Q$ is as per sequential circuit design and its state table.
Hold Time

- Hold time, $\bar{t}_h$ is an average of the minimum required time for input to hold its logic state unchanged after an enabling input (gate input or clock input) is applied so that the output $Q$ is as per the circuit design and its state table.
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Flip-Flop means a digital circuit of two stable states at an output:

1 means, rise on top. It means Flip, and 0 means fall to ground. It means flop.

Stable state can change only after a clock input applies.
FF output Q along with its complement \( \bar{Q} \)

- A particular combination of Q and \( \bar{Q} \) represents a stable state.
- An FF is also called a bistable digital circuit. One of the stable state is \( Q = 1 \) and \( \bar{Q} = 0 \), and other stable state is \( Q = 0 \) and \( \bar{Q} = 1 \).
- An FF has one or two inputs and clock edge. The logic states at these inputs and the previous Q determine what shall be the current outputs.
FF

• FF can have two definite (discrete) states.
• FF forms a smallest basic memory unit or a one-bit register unit
Present state feedbacks for next state

- Interconnections as well feedbacks are inputs
- Feedbacks are from outputs, Q and/or \( \overline{Q} \)
- Logic states at these inputs and the previous Q determine what shall be the current outputs
State table of flip-flop (FF)

- Describes how for the different input present and past conditions, the output Q (and/or $\bar{Q}$) shall be in given of FF after a clocking instance
A flip-flop has a feature that output should change only at a well defined instance of control input, called clock edge input.
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Latch

- A flip-flop is called latch, if the instance at which output should change has no well defined instances clock input.
- A latch is FF without no edge triggered clocking mechanism for its inputs.
- A latch may have a gating input (clock input interval) during which input changes affect changes in Q.
Summary
Sequential circuit output state depends not only on present input but on past state also.

For a sequential circuit, there is propagation delay, setup time and hold time.
• FF is a bistable circuit in which a timing input (called clock transition or clock edge input) controls the instance after which the output changes to next.

• A latch is a class of flip-flop in place of clock-edge instance at which output changes, a clock interval exists during which that output changes to next.
End of Lesson 2 on Sequential logic circuit, Flip Flop and Latch—Introduction
THANK YOU