Chapter 6

DIFFERENT TYPES OF LOGIC GATE
Lesson 5

ECL Gates
Outline

- Emitter coupled logic (ECL)
- ECL Circuit
- Characteristics of ECL gate circuit
- Wired OR case
- ECL Circuit features
- Circuit Parameters
ECL Input Stage and Basic Gate stage

- Each input of the gate gets the inputs at the base of the individual transistors, $T_A$, $T_B$.
- ECL basic gate is OR/NOR gate
ECL Input Stage and Basic Gate stage

- Each input of the gate gets inputs at the base of the individual transistors, $T_A$, $T_B$. The emitter of $T$ and $T_A$, $T_B$, couples together. [Hence the logic circuit name is emitter-coupled logic, ECL.]
- ECL basic gate is OR/NOR gate
Unconnected Input case

- If any input is not connected, the transistor $T_i$ base-emitter will be at cutoff. Therefore, it will be taken as low logic level.
There are ‘OR’ output stage transistor ($T_{OR}$) and ‘NOR’ output stage transistor ($T_{NOR}$). The outputs are taken from the emitters of each.

Collector of $T_{OR}$ connects to GND in the common collector amplifier mode (also called emitter-follower mode). The emitter gives the output, which also connects to $V_{EE}$ through a resistance $R_{out}$ (~1.5kΩ).
Collector of $T_{NOR}$ connects to GND in the common collector amplifier mode. The emitter gives the output, which also connects to $V_{EE}$ through a resistance $R'_{out}$ (~1.5kΩ).
Differential Amplifier

- There is transistor T, which forms a differential amplifier pair between T and the parallel circuits of $T_A$, $T_B$. The T gets the input reference voltage ($V_{REF} = -1.15V$) from a reference supply circuit. The pairs amplify the difference in the voltages (base currents) between the voltages at the bases of $T_A$, $T_B$, and reference voltage.
Differential Amplifier

- The emitters of the differential amplifier pairs connect through a common resistance $R_E (~1.18k\Omega)$ and to the –ve of supply’ $V_{EE} (~ -5V)$
Emitter follower (Common Collector) Amplifier

- The collectors of \( (T_A, T_B, \ldots) \) are also common. Common-collectors of the differential amplifier pairs connect through a resistance \( R_{C1} \) (~267Ω) to the GND (+ve with respect to the –ve supply).
Outline

- Transistor transistor logic (ECL)
- **ECL Circuit**
- Characteristics of ECL gate circuit
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Three Input ECL NOR Circuit with NPN Transistors

\[ V_R = -1.5V \]
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OR/NOR 3-INPUT
Output at $Y$ or $\overline{Y}$

- A common output from the transistor $T_{OR}$ at $Y$ or $T_{NOR}$ at $\overline{Y}$ is given to one (or more) next input n-p-n junction base of ECL stage(s) transistor.
Outline

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• **Wired OR case**
• ECL Circuit features
• Circuit Parameters
Wired ‘OR’

Circuit-1

A
B
C

ECL T_{NOR}

Circuit-2

A'
B'
C'

ECL T_{OR}

F
Wired OR Two ECL gates

- Y of ECL 1 interconnected to Y of ECL 2, the output can be considered as OR operation between the logic outputs
- \( F = (A + B + C) + (A' + B' + C') \)
Outline

- Transistor transistor logic (ECL)
- ECL Circuit
- Characteristics of ECL gate circuit
- Wired OR case

**ECL Circuit features**
- Circuit Parameters
Fast speed of operation

- Faster speed (2 ns propagation delay) of operation than TTL (10 ns), 74S TTL (3 ns)
- More power dissipation (50 mW/gate) than TTL (10 mW), 74S (19 mW)
Outline

- Transistor transistor logic (ECL)
- ECL Circuit
- Characteristics of ECL gate circuit
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- ECL Circuit features
- Circuit Parameters
Standard ECL 10k Series
Parameters

- Supply $V_{EE} = -5.2V$ $V_{CC} = 0V$
- $V_{OL}$ (Voltage Output at logic ‘0’) = $-1.7V$
- $V_{OH}$ (Voltage Output at logic ‘1’) = $-0.9V$
- $V_{IL}$ (Voltage Input at logic ‘0’) = $-1.4V$
- $V_{IH}$ (Voltage Input at logic ‘1’) = $-1.2V$
- $V_{TH}$ (Threshold Voltage) = $-1.29V$
ECL 10k Series Parameters

- Noise Margin at ‘1’or ‘0’output and input = 0.4V (–1.7V and –1.4V)
Summary
We learnt

• ECL gate circuit.
• ECL gate characteristics and parameters
• ECL gate features
• Faster speed (2 ns propagation delay) of operation than TTL (10 ns), 74S TTL (3 ns)
• More power dissipation (50 mW/gate) than TTL (10 mW), 74S (19mW)
We learnt

- ECL gate has each input connection to a base junction in an n-p-n transistor.
- ECL gate basic circuit is OR/NOR.
- ECL gate output can be Wired OR
End of Lesson 5

ETL Gate
THANK YOU