Chapter 6

DIFFERENT TYPES OF LOGIC GATES
Lesson 2

Characteristics of a Gate
Outline

• **Fan Out**

• Propagation Delay

• Wired Logic (Wired AND or Implied End) Connection

• Operational Voltage levels, Threshold Logic Input Voltage Noise margin

• Power Dissipation Per Gate

• Speed and Maximum operating Frequency
Fan out

- Number of logic gates at the next stage(s) — loaded to a given logic gate output so that voltages for each of the possible logic states (1 and 0) remain within the defined limits.
Examples — Limits for the gate connections

- Between $V_{oH}$ minimum and $V_{CC}$
- $V_{oL}$ maximum and $V_{EE}$

- Between $V_{oH} = \text{minimum}$
  
  \[ = 0.66 \times (V_{SS}^- - V_{SS}^-) \text{, and } V_{DD}^+ \]

- $V_{oL}$ maximum
  
  \[ = 0.33 \times (V_{SS}^- - V_{SS}^-) \text{ and } V_{SS}^- \]
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Propagation Delay

- Time interval between change in a defined reference point input voltage and reflection of its effect at the output.
- Time interval between changes in a defined logic level input and reflection of its effect at the output logic level.
Propagation Delay

- Slightly different values of the delays — when the input change from ‘0’ to ‘1’ and change from ‘1’ to ‘0’.
- Average propagation delay.
- Subject to variations in power supply and temperature — define a statistical deviation in delay and an average delay.
Outline

- Fan Out
- Propagation Delay
- **Wired Logic (Wired AND or Implied AND)**
- Connection
- Operational Voltage levels, Threshold Logic
- Input Voltage Noise margin
- Power Dissipation Per Gate
- Speed and Maximum operating Frequency
Wired ‘AND’

- When an output F can be obtained from joining together outputs of two or more gate circuits, then outputs gates when connected, the output is an AND operation between the logic outputs, and the joined circuit is called Wired AND circuit and the logic operation is called wired AND logic or Implied AND logic.
Wired ‘AND’

- Let an output $F$ is after joining by wire outputs of gate circuit-1 having inputs $A$ and $B$ and gate circuit-2 having inputs $C$ and $D$, then the joined circuit is called Wired AND circuit if

$$F = \frac{(A + B + C + D)}{.} = (A + B). (C + D)$$
Wired ‘AND’

Circuit-1

Circuit-2

Permitted
Example

- When any of the output of two or more circuits correspond to the saturation condition ~0.2V of transistor (meaning logic 0), the output from common point will become 0.2V. AND logic operation also means that any input 0 makes the output 0.

- Hence two transistors logic outputs gives wired AND in case above is true.
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Logic 0 Voltage levels

- A logic level ‘0’ at output is defined by voltage levels $V_{OL \text{max}}$ and $V_{OL \text{min}}$. A logic level ‘0’ at input is defined by voltage levels $V_{IL \text{max}}$ and $V_{IL \text{min}}$. 
Logic 1 Voltage levels

- A logic level ‘1’ at output is defined by voltage levels $V_{OH}$ maximum and $V_{OH}$ minimum. A logic level ‘1’ at input is defined by voltage levels $V_{IH}$ maximum and $V_{IH}$ minimum.
Threshold Voltage level

- A voltage where the transistor or MOSFET in the circuit changes the mode of working between saturation and cutoff. Actually used logic 0 or 1 operational voltage inputs should be specified above to ensure correct performance and should be sufficiently below threshold or above threshold.
Noise Margin at 0

• Noise margin for the logic output ‘0’ means the permitted worst case Voltage levels variations of the logic output ‘0’ when an output from a stage is the input at the next stage(s).
Noise Margin at 0 and at 1

- Noise margin for the logic output ‘1’ means the permitted worst case Voltage levels variations of the logic output ‘1’ when an output from a stage is the input at the next stage(s).
Permitted Noise Margins at 0 and 1

- The margins are permitted due to expected internal temperature variations and power supply variations. Permitted noise margins reflects the digital circuit immunity and worst case performance consistency in the presence of an induced noise.
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- **Power Dissipation Per Gate**
- Speed and Maximum operating Frequency
Power Dissipation per Gate

- How much average power dissipates per gate when a logic circuit is operated within the specified operating frequency
Power Dissipation per Gate per MHz

- How much average increase in values of power dissipates per gate when input frequency is increased by 1 MHz provided logic circuit is operated within the specified operating frequency maximum value.
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- \textbf{Speed and Maximum operating Frequency}
Speed

- How many times per second, a logic gate is able to respond to the change in the inputs and give the output as per specified logic
Operating frequency Maximum

- How many times logic levels changes per second are permitted without affecting the logic gate characteristics outside the limits, which have been set for the propagation delays, voltage levels and power dissipation per gate.
Summary
Two types of timer-counter devices -

- start, stop, reset and preloading a count programmable
- Free running timer-counter: start, stop, reset and preloading counts x, each one not programmable
Pre-scaling of timer-counter device -

- Programmable in TCNT 68HC11
- Programmable as 32 in mode-0 at T1 or T0 in 8051
- Pre-scaling delays the overflow rates and delays increment of counts by the pre-scaling factor
Overflow interrupt(s) of timer-counter device -

- Initiate an action
- Initiate an action after pre-fixed number of overflows
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End of Lesson 2

Characteristics of a Gate
THANK YOU